EAST SEARCH

8/8/05

L#	Hits	Search String	Databases
S1	2	5,465,216.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	2	5,513,122.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	2	5,859,962.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	2	5,901,073.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	2	5,913,022.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	2	5,905,883.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	2	5,937,183.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	2	5,966,516.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	2	5,974,575.pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	4367	((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	375	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (function$1 v	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	18	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (function$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	15	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (function$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	4371	((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	28	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (circuit with t	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	16	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state spac	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	27	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable w	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	2	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable \	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	2	(((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state spa	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	0	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (consequen	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	7	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (consequent	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	0	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable \	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	15	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (successive	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	4	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable \	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	2	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state spac	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	48	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (successive	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	29	(((digital or integrated) adj circuit) with simulat$3) and ("state space")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	69	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state space	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

09/630348 Yu-Chin Hsu

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Results of search set L10:(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (circuit with transition$1 with edge$1)

Document	Kind Codes	Title	Issue Date	Current OR	Abstract

US 20030192014 A1	Simulator of dynamic circuit for silicon critical path debug	20031009	716/4
US 20030179025 A1	Delay lock loop having an edge detector and fixed delay	20030925	327/158
US 20030149924 A1	Method and apparatus for detecting faults on integrated circuits	20030807	714/726
US 20030128022 A1	Method of testing an integrated circuit by simulation	20030710	324/121E
US 20030036893 A1	Method and apparatus for simulating transparent latches	20030220	703/16
US 20020109535 A1	Power on reset circuit arrangement	20020815	327/143
US 20020036539 A1	Post-silicon methods for adjusting the rise/fall times of clock edges	20020328	327/566
US 20020035708 A1	Method and apparatus for generating test patterns used in testing semiconductor integrated ci	20020321	714/25
US 20020011827 A1	Fault simulation method and fault simulator for semiconductor integrated circuit	20020131	324/71.5
US 20010037421 A1	Enhanced highly pipelined bus architecture	20011101	710/305
US 20010027549 A1	Method and apparatus for testing the timing of integrated circuits	20011004	714/734
US 6593765 B1	Testing apparatus and testing method for semiconductor integrated circuit	20030715	324/765
US 6532574 B1	Post-manufacture signal delay adjustment to solve noise-induced delay variations	20030311	716/6
US 6496953 B1	Calibration method and apparatus for correcting pulse width timing errors in integrated circuit	20021217	714/744
US 6493659 B1	Power consumption calculating apparatus and method of the same	20021210	703/14
US 6461882 B2	Fault simulation method and fault simulator for semiconductor integrated circuit	20021008	438/17
US 6407602 B1	Post-silicon methods for adjusting the rise/fall times of clock edges	20020618	327/170
US 6331800 B1	Post-silicon methods for adjusting the rise/fall times of clock edges	20011218	327/566
US 6289476 B1	Method and apparatus for testing the timing of integrated circuits	20010911	714/718
US 6148436 A	System and method for automatic generation of gate-level descriptions from table-based desc	20001114	716/18
US 6059450 A	Edge transition detection circuitry for use with test mode operation of an integrated circuit mer	20000509	714/724
US 6009531 A	Transition analysis and circuit resynthesis method and device for digital circuit modeling	19991228	713/400
US 5959485 A	Controllable one-shot circuit and method for controlling operation of memory circuit using sam	19990928	327/227
US 5649176 A	Transition analysis and circuit resynthesis method and device for digital circuit modeling	19970715	713/400
US 5600787 A	Method and data processing system for verifying circuit test vectors	19970204	714/30
US 5486783 A	Method and apparatus for providing clock de-skewing on an integrated circuit board	19960123	327/147
US 4949341 A	Built-in self test method for application specific integrated circuit libraries	19900814	714/736
US 6059450 A	Test mode initializing and verification method for integrated circuit memory device, involves in	20000509	

Results of search set S29:

US 20050125757 A1	Derivation of circuit block constraints	20050609	716/7
US 20050081169 A1	Measure of analysis performed in property checking	20050414	716/5
US 20040261043 A1	Integrated design verification and design simplification system	20041223	716/4
US 20040243880 A1	System for facilitating coverage feedback testcase generation reproducibility	20041202	714/25
US 20040216023 A1	Method and apparatus for maximizing and managing test coverage	20041028	714/742
US 20040199887 A1	Determining one or more reachable states in a circuit using distributed computing and one or	20041007	716/5
US 20040168137 A1	Use of time step information in a design verification system	20040826	716/5
US 20040163059 A1	Method and system for entropy driven verification	20040819	716/5
US 20040143800 A1	Method and apparatus for modeling dynamic systems	20040722	716/3
US 20040107409 A1	Automatic symbolic indexing methods for formal verification on a symbolic lattice domain	20040603	716/5
US 20040107174 A1	Parametric representation methods for formal verification on a symbolic lattice domain	20040603	707/1
US 20040103378 A1	System and method for building a binary decision diagram associated with a target circuit	20040527	716/3
US 20040098682 A1	Reachabilty-based verification of a circuit using one or more multiply rooted binary decision di	20040520	716/5

US 20040093572 A1	System and method for executing image computation associated with a target circuit	20040513 716/5
US 20040093571 A1	Circuit verification	20040513 716/5
US 20040093570 A1	System and method for verifying a plurality of states associated with a target circuit	20040513 716/5
US 20040093541 A1	System and method for evaluating an erroneous state associated with a target circuit	20040513 714/724
US 20040078673 A1	System and method for facilitating coverage feedback testcase generation reproducibility	20040422 714/33
US 20040064794 A1	Symbolic model checking with dynamic model pruning	20040401 716/2
US 20040030414 A1	Method and apparatus for automatic synthesis of controllers	20040212 700/1
US 20040015799 A1	Method of verifying and representing hardware by decomposition and partitioning	20040122 716/5
US 20030208730 A1	Method for verifying properties of a circuit model	20031106 716/4
US 20030188224 A1	System and method for facilitating programmable coverage domains for a testcase generator	20031002 714/25
US 20030187853 A1	Distributed data storage system and method	20031002 707/10
US 20030126059 A1	Intelectual property (IP) brokering system and method	20030703 705/36R
US 20030018461 A1	Simulation monitors based on temporal formulas	20030123 703/14
US 20020183990 A1	Circuit simulation	20021205 703/2
US 20020161564 A1	Method for modeling a reflected electrical wave in a digital simulation	20021031 703/13
US 20020138812 A1	Method of circuit verification in digital design	20020926 716/5
US 20020124208 A1	Method and system for reducing the computation tree to include only model behaviors defined	20020905 714/37
US 20020123867 A1	Sharing information between instances of a propositional satisfiability (SAT) problem	20020905 703/2
US 20020095645 A1	Searching for counter-examples intelligently	20020718 716/4
US 20010010091 A1	Method and apparatus for maximizing test coverage	20010726 716/4
US 6918099 B2	Method and system for entropy driven verification	20050712 716/4
US 6904578 B2	System and method for verifying a plurality of states associated with a target circuit	20050607 716/5
US 6892171 B2	Method for modeling a reflected electrical wave in a digital simulation	20050510 703/13
US 6848088 B1	Measure of analysis performed in property checking	20050125 716/4
US 6782518 B2	System and method for facilitating coverage feedback testcase generation reproducibility	20040824 716/5
US 6728939 B2	Method of circuit verification in digital design	20040427 716/5
US 6643827 B1	Symbolic model checking with dynamic model pruning	20031104 716/2
US 6609229 B1	Method for automatically generating checkers for finding functional defects in a description of	20030819 716/4
US 6587998 B2	Searching for counter-examples intelligently	20030701 716/5
US 6564194 B1	Method and apparatus for automatic synthesis controllers	20030513 706/13
US 6560758 B1	Method for verifying and representing hardware by decomposition and partitioning	20030506 716/7
US 6484134 B1	Property coverage in formal verification	20021119 703/14
US 6408424 B1	Verification of sequential circuits with same state encoding	20020618 716/5
US 6349272 B1	Method and system for modeling time-varying systems and non-linear systems	20020219 703/2
US 6339837 B1	Hybrid method for design verification	20020115 716/5
US 6321186 B1	Method and apparatus for integrated circuit design verification	20011120 703/15
US 6321184 B1	Reduction of arbitrary L1-L2 circuits for enhanced verification	20011120 703/15
US 6314553 B1	Circuit synthesis and verification using relative timing	20011106 716/18
US 6311293 B1	Detecting of model errors through simplification of model via state reachability analysis	20011030 714/37
US 6247163 B1	Method and system of latch mapping for combinational equivalence checking	20010612 716/3
US 6212669 B1	Method for verifying and representing hardware by decomposition and partitioning	20010403 716/7
US 6175946 B1	Method for automatically generating checkers for finding functional defects in a description of	20010116 716/4
US 6106567 A	Circuit design verification tool and method therefor using maxwell's equations	20000822 716/5
US 6049662 A	System and method for model size reduction of an integrated circuit utilizing net invariants	20000411 703/16

US 5999717 A	Method for performing model checking in integrated circuit design	19991207	703/2
US 5917917 A	Reduced-memory reverberation simulator in a sound synthesizer	19990629	381/63
US 5910897 A	Specification and design of complex digital systems	19990608	716/19
US 5764952 A	Diagnostic system including a LSI or VLSI integrated circuit with a diagnostic data port	19980609	716/4
US 5680332 A	Measurement of digital circuit simulation test coverage utilizing BDDs and state bins	19971021	703/13
US 5657283 A	Diagnostic data port for a LSI or VLSI integrated circuit	19970812	365/201
US 5544107 A	Diagnostic data port for a LSI or VLSI integrated circuit	19960806	365/201
US 5493508 A	Specification and design of complex digital systems	19960220	716/5
US 5491639 A	Procedure for verifying data-processing systems	19960213	716/5
EP 1221663 A2	A method of circuit verification in digital design	20020710	
US 20040143800 A	Simulation program with integrated circuit emphasis modeling system generates schematic of	20040722	
US 20040123254 A	Method for verifying complete model of design system such as integrated circuits, involves re:	20040624	